REMARKS

Reconsideration of the present application is respectfully requested. Claims 1-29 previously presented for examination remain in the application. Claims 1, 19 and 22 have been amended to place the claims in better form for consideration on appeal and to more clearly state and distinctly claim the features that applicant regards as an embodiment of the invention. No new claims have been added and no claims have been canceled.

Claims 1-29 stand rejected under 35 U.S.C. § 102(b) as being considered to be anticipated by U.S. Patent No. 5,159,690 to Margolus et al. ("Margolus").

Claim 1 includes the limitations

> 1. A processor comprising:
> a first memory to store instructions and data for use by the processor, the first memory further to store data representing a first state of a cellular automaton at a first time step, the data to be organized in cells;
> a first update engine, the first update engine including a microprocessor execution unit capable of executing general purpose microprocessor instructions; and
> a cellular automaton update unit to provide data from selected cells of the cellular automaton to the first update engine,
> the first update engine to update at least some of the selected cells according to an update rule and a state of any associated neighborhood cells to provide a state of the cellular automaton at a second time step, the first memory, the first update engine and the cellular automaton update unit being integrated on a single chip.

(Claim 1)(emphasis added).

Applicant respectfully submits that Margolus fails to teach or suggest at least a single integrated circuit chip capable of storing and updating data representing a cellular automaton as previously argued. In particular, Margolus

fails to teach or suggest a general-purpose microprocessor execution unit that also updates cellular automata data.

As previously discussed, Margolus discloses a computer system and approach for coordinating the activity of multiple processors to permute stored data elements and apply transformation rules to permuted elements. (see e.g. Margolus, Abstract). Margolus refers to the use of multiple processors and memory components to store and update cellular automata data. As described in Margolus, the processors of Margolus are actually large static-RAM lookup tables. (col. 9, lines 1-2).

Margolus does not teach or suggest storing and updating cellular automata data using a single chip including at least a microprocessor execution unit capable of executing at least some general-purpose microprocessor instructions.

It is stated in the office action that the Examiner believes that integration on a single chip no longer provides a patentable distinction. It is further stated that the processors in the reference clearly execute microprocessor instructions.

Applicant respectfully traverses these remarks. The presently presented claims set forth one or more features relating to a microprocessor execution unit capable of executing microprocessor instructions. As stated above, the processors of Margolus are implemented using SRAM look-up tables. Margolus does not teach the use of a microprocessor and thus, cannot be considered to teach the use of a microprocessor execution unit.

For at least these reasons, claim 1 is patentably distinguished over Margolus.

Independent claims 11, 19, and 22 include a similar limitation. Claims 2-10, claims 12-18, claims 20-21 and claims 22-29 depend from and further limit claims 1, 11, 19 and 22, respectively, and thus, should be found to be patentably distinguished over Margolus for at least the same reasons.

Based on the foregoing, applicants respectfully submit that the applicable rejections have been overcome and that claims 1-29 are in condition for allowance.

If the Examiner disagrees or believes that further discussion will expedite prosecution of this case, the Examiner is invited to telephone applicant's representative Cynthia Thomas Faatz at (408) 765-2057.

If there are any charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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